REMARKS/ARGUMENTS

Claims 1-11 and 28-42 are pending.

Claims 1-4, 7-11, 28-36, and 39-41 were rejected under 35 U.S.C. § 102(b) for allegedly being anticipated by Barth et al., U.S. Patent No. 5,747,914.

Claims 1-11 and 28-41 were rejected under 35 U.S.C. § 103(a) for allegedly being unpatentable over Dosaka et al., U.S. Patent No. 5,680,363 in view of Kundu, U.S. Patent No. 5,692,148.

Section 102 Rejection of Claim 1

Claim 1, as amended, recites in part "a symmetrical layout along a horizontal direction" including a left memory portion, a central single row cache, and a right memory portion. Moreover, the recited elements comprising the left portion are also "arranged along the horizontal direction," as are the recited elements of the right memory portion. Thus, all the recited elements lie along the horizontal direction. This recited feature of claim 1 is shown in Fig. 1 of the pending specification; no new matter has been added.

Although Fig. 7 of Barth et al. shows a left portion, a decoder (718), and a right portion arranged along a horizontal direction, the left portion elements (702A, 704, 708A) are NOT arranged in the horizontal direction. Similarly, the right portion elements (702B, 706, 708B) are NOT arranged in the horizontal direction. Rather, it is clear that the left and right portions are arranged vertically with respect to the horizontal direction. The structure of Barth et al. does not anticipate claim 1, and for at least this reason, the Section 102 rejection of claim 1 is overcome.

Claim 1 additionally recites in part "one centrally located single row cache ... disposed between said left plurality of memory portions and said right plurality of memory portions." Barth et al. do not show "one" single row cache between left and right portions. In fact, Fig. 6 cited by the examiner clearly shows two caches (604, 608) as disclosed in column 5, lines 58-61. As to Fig. 7, there is no description as the configuration of the cache. Barth et al. therefore do not show "one centrally located single row cache ... disposed between said left

plurality of memory portions and said right plurality of memory portions," and for at least this reason the Section 102 rejection of claim 1 is overcome.

Claim 1 additionally recites in part "receiving an initial command that is not a 'read' command" which specifies a row and is "exclusive of column address data," and then "moving said contents of said row into said single row cache." Barth et al. disclose at column 6, lines 22-36 a request packet containing a storage location and an operation to be performed on the storage location. Barth et al. then describe a read operation in which data is accessed from the storage location and then read out; the read operation clearly includes "the column that corresponds to the address contained in the request packet." *Col. 6, lines 34-35.* Barth et al. therefore do not describe "receiving an initial command that is not a 'read' command" which is "exclusive of column address data." For at least this reason, the Section 102 rejection of claim 1 is overcome.

Claim 1 further recites in part "after said contents of said row have been moved into said single row cache, receiving a 'read' command and column address data." Barth et al. clearly explain that the row of data is read out during a read operation. *Col. 6, lines 27-31.* Barth et al. do not show data having already been read into cache memory, and then receiving a read command. For at least this reason, the Section 102 rejection of claim 1 is overcome.

Section 102 Rejection of Claim 28

Claim 28 as amended recites in part "a single cache ... to latch a selected row of data read out from the first memory blocks or a selected row of data read out from the second memory blocks." Barth et al. do not show "a single cache" as recited in claim 28. As discussed above, Barth et al. show in Fig. 6 that each bank has its corresponding cache. (604, 608). This is not the recited "single cache ... to latch a selected row of data read out from the first memory blocks or a selected row of data read out from the second memory blocks." For at least this reason, the Section 102 rejection of claim 28 is overcome.

Claim 28 further recites in part "wherein an entire row of data from the first memory blocks is stored in the row cache in response to receiving a 'bank activate' command, the 'bank activate' command absent a column address." Barth et al. clearly does not show a 'bank

activate' command that is "absent a column address" or that "an entire row of data from the first memory blocks is stored in the row cache in response to receiving a 'bank activate' command." Instead, Barth et al. discloses a read operation that includes "the column that corresponds to the address contained in the request packet." *Col. 6, lines 34-35.* This is not the recited "bank activate command." For at least this reason, the Section 102 rejection of claim 28 is overcome.

Claim 28 further recites in part "a column decoder to access data stored in the row cache in response to receiving a 'read' command subsequent to receiving the 'bank activate' command, the 'read' command including a column address." Barth et al. disclose performing a read operation. *Col. 6, lines 27-36.* Barth et al. do not describe "receiving a 'read' command subsequent to receiving the 'bank activate' command." For at least this reason, the Section 102 rejection of claim 28 is overcome.

The examiner noted that "bank activation and precharging are also present in conventional DRAMs." *O.A. Paragraph 4 in Detailed Action.* While the idea of "bank activation" is known, claim 28 recites "wherein an entire row of data from the first memory blocks is stored in the row cache in response to receiving a 'bank activate' command" which is not known. The examiner is required to show wherein the cited references this particular recited limitation is shown.

Section 102 Rejection of Claim 39

Claim 39 recites in part limitations similar to the limitations discussed in connection with claim 28. The Section 102 rejection of claim 39 is therefore believed to be overcome for any one of the reasons set forth in the above discussion of claim 28.

Section 103 Rejection of Claim 1

Claim 1 recites in part "one centrally located single row cache ... disposed between said left plurality of memory portions and said right plurality of memory portions." Dosaka et al. do not show "one" single row cache between left and right portions. In fact, Fig. 22 cited by the examiner clearly shows no less that four caches (SMA_1-SMA_4). Moreover, these are SRAM array blocks. *Col. 34, lines 26-27.* These caches therefore do not show or even

suggest "one centrally located single row cache ... disposed between said left plurality of memory portions and said right plurality of memory portions."

The examiner also appears to have cited column 5, lines 11-13. Fig. 27 shows a cache register (506). However, Fig. 27 does not show or suggest a single cache "disposed between said left plurality of memory portions and said right plurality of memory portions." Thus, neither Dosaka's Fig. 22 nor Dosaka's prior device of Fig. 27 show or suggest "one centrally located single row cache ... disposed between said left plurality of memory portions and said right plurality of memory portions." For at least this reason, the Section 103 rejection of claim 1 is believed to be overcome.

Claim 1 additionally recites in part "receiving an initial command that is not a 'read' command and ... receiving row address data for reading contents of a row of said synchronous memory, said initial command exclusive of column address data." Column 13, lines 28-30 (discussion of Fig. 1) was cited for showing "receiving an initial command." This cite is part of a discussion relating to the movement of data into SRAM (2) after the data has already been read out of the DRAM, the explanation of which is given in column 11, line 66 to column 12, line 33. In that discussion, Dosaka discloses reading out a row of data from the DRAM based on an external address that contains row address and the column address ("generates the internal column address signal from the external address", *col. 12, lines 21-22*). The examiner's cited column 13, lines 28-30 therefore does not show the recited "receiving an initial command that is not a 'read' command and ... receiving row address data for reading contents of a row of said synchronous memory, said initial command exclusive of column address data" because the discussion given at this portion of Dosaka already presumes the row of data has been read out of the DRAM (including receiving an external address that contains both row and column addresses).

Claim 1 additionally recites receiving a read command after "moving said contents of said row into said single row cache." Dosaka clearly does not show this, despite the examiner's cite of column 5, lines 11-13 and 20-23. Though col. 5, lines 11-13 describes transferring data between one row in the memory cell array and the SRAM array, this does not read the recited receiving a read command after "moving said contents of said row into said

single row cache" because in Dosaka the transfer is the result of a read command; i.e., the transfer follows the read command. In contrast, the claim recites a read command following the transfer.

Dosaka does not teach or suggest the foregoing discussed limitations, and so the Section 103 rejection of claim 1 is believed to be overcome.

Section 103 Rejection of Claim 28

Claim 28 further recites in part "a column decoder to access data stored in the row cache in response to receiving a 'read' command subsequent to receiving the 'bank activate' command, the 'read' command including a column address." The examiner has not directly addressed this limitation in his Section 103 rejection of 28. The examiner is required to show where in the Section 103 references this limitation is shown.

Claim 28 recites in part "wherein an entire row of data from the first memory blocks is stored in the row cache in response to receiving a 'bank activate' command, the 'bank activate' command absent a column address." The examiner has not directly addressed this limitation in his Section 103 rejection of 28. However, in his Section 103 rejection of claims 2-4, 7-10, 32, 33, 35, and 36, the examiner states "bank activation and precharging are also present in conventional DRAMs." While the idea of "bank activation" is known, claim 28 recites "wherein an entire row of data from the first memory blocks is stored in the row cache in response to receiving a 'bank activate' command" which is not known. The examiner is required to show where in the Section 103 references this particular limitation is shown.

For at least these reasons, the Section 103 rejection of claim 28 is believed to be overcome.

Section 103 Rejection of Claim 39

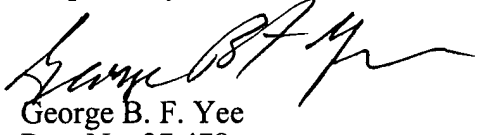
Claim 39 recites in part limitations similar to the limitations discussed in connection with claim 28. The Section 103 rejection of claim 39 is therefore believed to be overcome for the reasons set forth in the above discussion of claim 28.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



George B. F. Yee
Reg. No. 37,478

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
GBFY:cmm
60632630 v1